Faculty of Computing



**Computer Architecture**

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**(LAB -03)**

**Instructor**

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**Half Adder Simulation in Proteus**

**Objective:**

To design and simulate a **Half Adder** circuit using Proteus, understand its functionality, and verify its truth table through practical implementation.

**Required Software:**

* Proteus Design Suite (Version 8 or later)

**Required Components:**

* XOR and AND gates (for Half Adder design)
* Logic Input (for input signals)
* Logic Output (to observe results)
* LED (for visual representation)
* Connecting wires
* Power and ground terminals
* Resistors (for current limiting)

**Introduction to Half Adder:**

A **Half Adder** is a basic combinational circuit used to add two binary numbers. It takes two inputs, performs the addition, and provides two outputs:

1. **Sum (S)** – Result of XOR operation between inputs.
2. **Carry (C)** – Result of AND operation between inputs.

**Boolean Expressions:**

* **Sum (S) = A ⊕ B** (XOR Gate)
* **Carry (C) = A . B** (AND Gate)

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Sum (A XOR B)** | **Carry (A AND B)** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Half Adder in Proteus:**

**Step-by-Step Procedure:**

1. **Open Proteus** and create a new project.
2. Click on **“P”** (Pick Device) and search for **XOR** and **AND** gates.
3. Place the **XOR and AND gates** on the schematic workspace.
4. Add **Logic Input components** to represent binary inputs A and B.
5. Connect:
   * **A and B to the XOR gate** (for Sum output).
   * **A and B to the AND gate** (for Carry output).
6. Attach **LEDs** to the outputs to visually indicate the results.
7. Add **resistors (330Ω)** in series with LEDs to prevent excessive current.
8. Provide **power and ground connections** to complete the circuit.
9. **Run the simulation** and test different input combinations to verify the truth table.

**Explanation of Components Used:**

* **XOR Gate:** Produces HIGH output (1) when inputs are different.
* **AND Gate:** Produces HIGH output (1) only when both inputs are HIGH.
* **Logic Inputs:** Used to provide binary signals (0 or 1) for simulation.
* **LEDs:** Used to visually indicate the circuit’s output.
* **Resistors (330Ω):** Used to limit current flow through the LEDs and prevent damage.
* **Power and Ground:** Necessary to provide the circuit with operating voltage and a return path for current.

**Observations:**

* Verify the truth table by testing all possible input combinations.
* Observe that the **Sum** LED lights up when inputs are different.
* Observe that the **Carry** LED lights up only when both inputs are HIGH.

**Troubleshooting Tips:**

* If LEDs do not light up, check the power and ground connections.
* Ensure correct wiring between XOR, AND gates, and LEDs.
* Verify that resistors are correctly placed to prevent LED damage.

**Conclusion:**

* Successfully designed and simulated a **Half Adder** circuit in Proteus.
* Understood how logic gates function to perform binary addition.
* Verified theoretical truth table with practical simulation results.

**Class Tasks:**

* 1. Design and simulate a simple NAND Gate using switches instead of logic states.
  2. Design and simulate XNOR Gate.
  3. Design and simulate a half Subtractor.